Two or more of the above method steps, examples, dimensions, etc. may be combined in the present invention, depending on for instance requirements of a final device, transistor, etc.

The invention claimed is:

1. A method of manufacturing a semiconductor III-V structure, comprising:

providing a substrate;

providing an active layer, by epitaxially growing a III-V semiconducting layer stack on top of the substrate, wherein epitaxially growing the III-V semiconducting layer stack comprises (i) growing a first active III-V layer and (ii) growing a second III-V active layer, thereby forming a two-dimensional electron gas between the first III-V active layer and the second III-V active layer;

providing a protection layer stack for use as a mask for the first III-V active layer and the second III-V active layer, wherein the protection layer stack comprises (i) a III-V evaporation layer, (ii) a III-V etch stop layer on top of the evaporation layer, and (iii) a dielectric mask layer on top of the etch stop layer;

locally etching the dielectric mask layer and the III-V etch stop layer in a gate region; and

evaporating the III-V evaporation layer in the gate region to expose the second III-V active layer, wherein the dielectric mask layer remains in a region outside the gate region after evaporating the III-V evaporation layer in the gate region.

2. The method of claim **1**, wherein the III-V evaporation layer comprises one or more of N, P, or As, and one or more of B, Al, Ga, In, or Tl, and wherein the evaporation layer has a thickness of 2 nm-10 nm.

3. The method of claim **1**, wherein the III-V etch stop layer comprises one or more of N, P, or As, and one or more of B, Al, Ga, In, or Tl.

4. The method of claim **1**, wherein the etch stop layer has a thickness of 0.3 nm-100 nm.

5. The method of claim **1**, wherein the dielectric mask layer comprises one or more of Si, Al, O, or N.

6. The method of claim **1**, wherein the dielectric mask layer has a thickness of 1 nm-500 nm.

7. The method of claim **1**, further comprising providing a gate through the protection layer stack, wherein (i) the gate comprises a p-type III-V material, and (ii) the gate is selectively and epitaxially re-grown in the gate region.

8. The method of claim **7**, further comprising forming an ohmic contact on the gate.

9. The method of claim **7**, wherein the gate being re-grown comprises the gate being re-grown by metal organic vapor phase epitaxy.

10. The method of **7**, wherein the gate comprises one or more of N, P, or As, and one or more of B, Al, Ga, In, or Tl.

11. The method of claim **7**, further comprising:

providing a photoresist mask on top of the dielectric mask layer.

12. The method of claim **7**, further comprising providing a source and a drain through the protection layer stack, (i) the source and drain comprise an n-type III-V material, and (ii) the source and drain are selectively and epitaxially re-grown.

13. The method of claim **12**, wherein an ohmic contact is formed on the source and drain.

14. The method of claim **12**, wherein the source and drain being re-grown comprises the source and drain being re-grown by metal organic vapor phase epitaxy.

15. The method of claim **12**, wherein the source and drain comprises one or more of N, P, or As, and one or more of B, Al, Ga, In, or Tl.

16. The method of claim **1**, wherein:

the substrate comprises a <111> silicon substrate;

the first active III-V layer is a III-N layer; and

the second active III-V layer is a III-N layer.

17. The method of claim **1**, wherein the first active III-V layer has a thickness of 20 nm-500 nm.

18. The method of claim **1**, wherein the second active III-V layer has a thickness of 10 nm-100 nm.

19. The method of claim **1**, wherein the first active III-V layer comprises one or more of N, P, or As, and one or more of B, Al, Ga, In, or Tl.

20. The method of claim **1**, wherein the second active III-V layer comprises one or more of N, P, or As, and one or more of B, Al, Ga, In, or Tl.

21. A semiconductor structure comprising:

an active layer comprising (i) a first active III-V layer and (ii) a second active III-V layer, wherein a two-dimensional electron gas is formed between the first active III-V layer and the second active III-V layer;

a protection layer stack configured for use as a mask, wherein the protection layer stack comprises (i) a III-V evaporation layer, wherein the evaporation layer has a thickness of 2 nm-10 nm, (ii) a III-V etch stop layer on top of the evaporation layer, and (iii) a dielectric mask layer on top of the etch stop layer; and

a gate, wherein (i) the gate comprises a p-type III-V material, and (ii) the gate is selectively and epitaxially re-grown in contact with the second active III-V layer.

22. The semiconductor structure of claim **21**, further comprising an ohmic contact formed on the gate.

23. The semiconductor structure of claim **21**, further comprising a source and a drain, wherein (i) the source and the drain comprise an n-type III-V material, and (ii) the source and the drain are selectively and epitaxially re-grown.

24. The semiconductor structure of claim **23**, further comprising an ohmic contact formed on the source and the drain.

25. The semiconductor structure of claim **21**, wherein the semiconductor structure is included within a transistor device.

26. The semiconductor structure of claim **21**, wherein the semiconductor device is included in an electronic circuit selected from the group consisting of a switch, a high-power application circuit, a high-voltage application circuit, an image sensor, a biosensor, an integrated logic circuit, and an ion sensor.

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